

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	22	(substrate semiconductor wafer silicon) and (etch\$6 same (hardmask (hard adj mask)) same (contact plug barrier) same encapsulat\$6 same (capacitor ((lower bottom first second upper top) adj electrode)))	US-PGPUB; USPAT	OR	ON	2005/09/26 10:24
L2	156	(substrate semiconductor wafer silicon) and (etch\$6 same (hardmask (hard adj mask)) same (contact plug barrier) same capacitor same ((lower bottom first second upper top) adj electrode))	US-PGPUB; USPAT	OR	ON	2005/09/26 09:21
L3	85	etch\$6 and (hardmask (hard adj mask)) and (contact plug barrier) and capacitor and ((lower bottom first second upper top) adj electrode)	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/26 09:33
L4	1316	encapsulat\$6 and (capacitor ((lower bottom first second upper top) adj electrode))	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/26 08:34
L5	70	L4 and (etch\$6 hardmask (hard adj mask))	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/26 09:38
L6	6387	438/3.ccls. 438/240.ccls. 438/253.ccls. 438/396.ccls. 257/532.ccls.	US-PGPUB; USPAT	OR	OFF	2005/09/26 08:35
L7	163	L6 and ((etch\$6 hardmask (hard adj mask)) same encapsulat\$6)	US-PGPUB; USPAT	OR	ON	2005/09/26 09:45
L8	345	L6 and (etch\$6 same (hardmask (hard adj mask)) same (electrode contact plug barrier encapsulat\$6))	US-PGPUB; USPAT	OR	ON	2005/09/26 10:01
L9	1766	438/3.ccls.	US-PGPUB; USPAT	OR	OFF	2005/09/26 08:35
L10	190	((substrate semiconductor wafer silicon) and (hardmask (hard adj mask)) and (capacitor ((lower bottom first second upper top) adj electrode))).clm.	US-PGPUB	OR	ON	2005/09/26 10:26
L11	118	((substrate semiconductor wafer silicon) and (hardmask (hard adj mask)) and (capacitor ((lower bottom first second upper top) adj electrode)) and (contact plug barrier encapsulat\$6)).clm.	US-PGPUB	OR	ON	2005/09/26 10:27